Amendments to the Claims:

This listing will replace all prior versions, and listing, of claims in the application.

1. (original) A method of creating an interface layer over the surface of a semiconductor device, comprising the steps of:

providing a semiconductor device, said semiconductor device having a first and a second surface with points of electrical contact to said semiconductor device having been provided in said second surface of said semiconductor device, said semiconductor device having been provided with a layer of passivation over said second surface of said semiconductor device, openings having been created through said layer of passivation exposing said points of electrical contact to said semiconductor device;

providing a semiconductor device mounting support having a first and a second surface, contact pads having been provided in said first or said second surface of said semiconductor device mounting support;

positioning said semiconductor device over the second surface of said semiconductor device mounting support, said

first surface of said semiconductor device facing said second surface of said semiconductor device mounting support;

providing conductive interconnections between said points of electrical contact provided in said second surface of said semiconductor device and contact pads provided over the second surface of said semiconductor device mounting support;

providing an underfill for said semiconductor device;

depositing an interface layer over the surface of said layer of passivation; and

patterning and etching said interface layer, creating at least one opening through said interface layer.

2. (original) The method of claim 1, said interface layer comprising polysilicon.

3. (original) The method of claim 1, further comprising depositing a layer of mold compound over the surface of said interface layer, filling said at least one opening created through said interface layer.

4. (original) A method of creating protective layers for the packaging of a semiconductor device, comprising the steps of:

providing a semiconductor device, said semiconductor device having a first and a second surface with points of electrical contact to said semiconductor device having been provided in said second surface of said semiconductor device, said semiconductor device having been provided with a layer of passivation over said second surface of said semiconductor device, openings having been created through said layer of passivation exposing said points of electrical contact to said semiconductor device;

providing a semiconductor device mounting support having a first and a second surface, contact pads having been provided in said first or said second surface of said semiconductor device mounting support;

positioning said semiconductor device over the second surface of said semiconductor device mounting support, said first surface of said semiconductor device facing said second surface of said semiconductor device mounting support;

providing conductive interconnections between said points of electrical contact provided in said second surface of said semiconductor device and contact pads provided over the second surface of said semiconductor device mounting support;

providing an underfill for said semiconductor device;

depositing an interface layer over the surface of said layer of passivation;

patterning and etching said interface layer, creating at least one opening through said interface layer; and

depositing a layer of mold compound over the surface of said interface layer, filling said at least one opening created through said interface layer.

5. (original) The method of claim 4, said interface layer comprising polysilicon.

Claims 6-10: (cancelled)

11. (currently amended) A method for applying a stress ~~relieve~~ relief interface layer over a semiconductor surface, comprising the steps of:

providing a semiconductor surface, said semiconductor surface comprising at least one completed semiconductor device, said at least one completed semiconductor device being densely packed and having a relatively large surface area;

depositing a stress ~~relieve~~ relief interface layer over said semiconductor surface; and

creating at least one opening through said stress ~~relieve~~ relief interface layer.

12. (original) The method of claim 11, said semiconductor surface being a surface of a semiconductor device.

13. (currently amended) The method of claim 11, said stress ~~relieve~~ relief interface layer ~~providing relieve to~~ relieving stress introduced by mismatched Coefficients of Thermal Expansion (CTE) of thermally interacting layers.

14. (currently amended) The method of claim 11, said stress ~~relieve~~ relief interface layer comprising polysilicon.

15. (currently amended) The method of claim 11, further comprising depositing a layer of mold compound over the surface of said stress ~~relieve~~ relief interface layer, filling said at least one opening created through said stress ~~relieve~~ relief interface layer.

16. (currently amended) A method for applying a stress ~~relieve~~ relief interface layer over a semiconductor surface, comprising the steps of:

providing a semiconductor surface;

depositing a stress ~~relieve~~ relief interface layer over said semiconductor surface;

creating at least one opening through said stress ~~relieve~~ relief interface layer; and

depositing a layer of mold compound over the surface of said stress ~~relieve~~ relief interface layer, filling said at least one opening created through said stress ~~relieve~~ relief interface layer.

17. (original) The method of claim 16, said semiconductor surface being a surface of a semiconductor device.

18. (currently amended) The method of claim 16, said stress ~~relieve~~ relief interface layer ~~providing relieve to~~ relieving stress introduced by mismatched Coefficients of Thermal Expansion (CTE) of thermally interacting layers.

19. (currently amended) The method of claim 16, said stress ~~relieve~~ relief interface layer comprising polysilicon.

20. (currently amended) A method for applying a stress ~~relieve~~ relief interface layer over a semiconductor surface, comprising the steps of:

providing a semiconductor surface, said semiconductor surface comprising at least one completed semiconductor device, said at least one completed semiconductor device being densely packed and having a relatively large surface area;

depositing a layer of polysilicon over said semiconductor surface; and

creating at least one opening through layer of polysilicon.

21. (original) The method of claim 20, said semiconductor surface being a surface of a semiconductor device.

22. (currently amended) The method of claim 20, said layer of polysilicon ~~providing relieve to~~ relieving stress introduced by mismatched Coefficients of Thermal Expansion (CTE) of thermally interacting layers.

23. (original) The method of claim 20, further comprising depositing a layer of mold compound over the surface of said layer of polysilicon, filling said at least one opening created through said layer of polysilicon.

24. (currently amended) A method for applying a stress ~~relieve~~ relief interface layer over a semiconductor surface, comprising the steps of:

providing a semiconductor surface;

depositing a layer of polysilicon over the surface of said semiconductor surface;

creating at least one opening through said layer of polysilicon; and

depositing a layer of mold compound over the surface of said layer of polysilicon, filling said at least one opening created through said layer of polysilicon.

25. (original) The method of claim 24, said semiconductor surface being the surface of a semiconductor device.

26. (currently amended) The method of claim 24, said layer of polysilicon ~~providing relieve to~~ relieving stress introduced by mismatched Coefficients of Thermal Expansion (CTE) of thermally interacting layers.

27. (currently amended) A method for applying a stress ~~relieve~~ relief interface layer over a semiconductor surface, comprising the steps of:

providing a semiconductor device;

depositing a layer of polysilicon over a surface of said semiconductor device; and

creating at least one opening through layer of polysilicon.

28. (currently amended) The method of claim 27, said layer of polysilicon ~~providing relieve to~~ relieving stress introduced by mismatched Coefficients of Thermal Expansion (CTE) of thermally interacting layers.

29. (original) The method of claim 27, further comprising depositing a layer of mold compound over the surface of said layer of polysilicon, filling said at least one opening created through layer of polysilicon.

30. (currently amended) A method for applying a stress ~~relieve~~ relief interface layer over a semiconductor surface, comprising the steps of:

providing a semiconductor device;

depositing a layer of polysilicon over a surface of said semiconductor device;

creating at least one opening through said layer of polysilicon; and

depositing a layer of mold compound over the surface of said layer of polysilicon, filling said at least one opening created through said layer of polysilicon.

31. (currently amended) The method of claim 30, said layer of polysilicon ~~providing relieve to~~ relieving stress introduced by mismatched Coefficients of Thermal Expansion (CTE) of thermally interacting layers.